TVW ST23 04 AD0 Engineering Specification

1. Scope

TVW ST23 04 AD0's are TVS arrays designed to protect high-speed signal lines from overvoltage hazard of Electrostatic Discharge (**ESD**), Electrical Fast Transients (**EFT**) and **Lightning**. These interfaces can be used in **HDMI**, **DisplayPort** interface, SATA and eSATA interface, digital visual interface (DVI), USB2.0, IEEE 1394 Firewire Ports, Ethernet port (10/100/1000 Mb/s), etc.

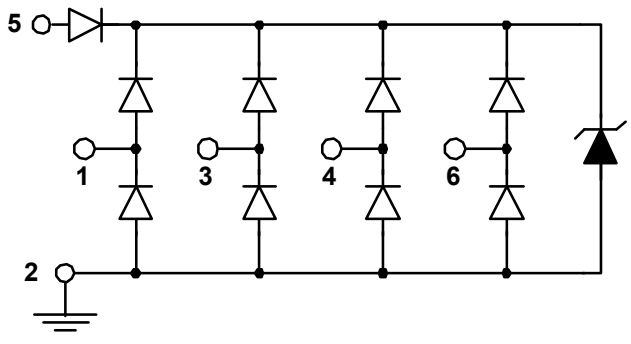
TVW ST23 04 AD0 incorporates a pair of rail-to-rail diodes with ultra low capacitance for each of four I/O channels. Additional Zener diode is employed to minimize the influence of supply voltage. The ESD protection of TVS arrays meets the immunity standard of IEC 61000-4-2, level 4 (±15kV air, ±8kV contact discharge).

2. Explanation of Part Number

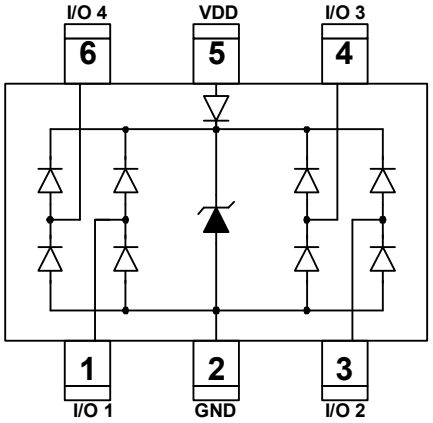
TV	**W**	**ST23**	**04**	**AD0**
(1)	(2)	(3)	(4)	(5)

(1) Product Type：TV=TVS Diode
(2) Capacitance Code：W=Ultra Low Capacitance
(3) Package Size Code
(4) Channel Code：04=4 Channels
(5) Specialized Specification Code

3. Circuit Diagram /Pin Configuration



Circuit Diagram



Pin Configuration
SOT23-6L (Top-view)

4. Specifications

4.1. ABSOLUTE MAXIMUM RATINGS

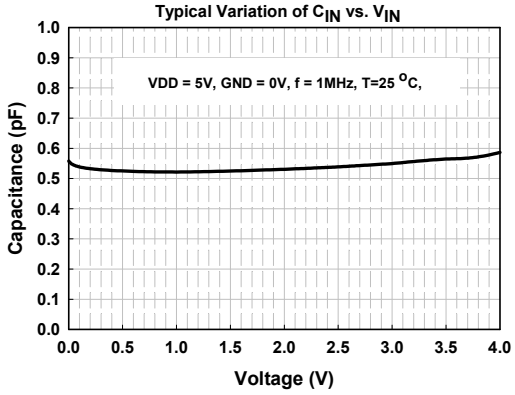
PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp =8/20μs) (I/O pins)	I_{PP}	4.7	A
Operating Supply Voltage (VDD-GND)	V_{DC}	6	V
ESD per IEC 61000-4-2 (Air) (I/O pins) ESD per IEC 61000-4-2 (Contact) (I/O pins)	V_{ESD_IO}	19 12	kV
ESD per IEC 61000-4-2 (Air) (VDD, GND pins) ESD per IEC 61000-4-2 (Contact) (VDD, GND pins)	V_{ESD_PW}	30 30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	V

4.2. ELECTRICAL CHARACTERISTICS

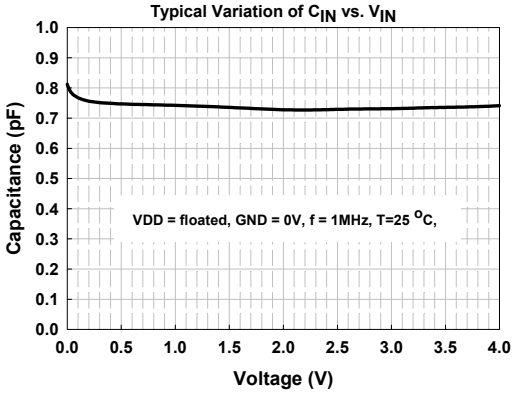
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to pin 2, T=25 °C			5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, Pin 5 to pin 2			5	μA
Channel Leakage Current	$I_{CH-Leak}$	V_{Pin5} = 5V, V_{Pin2} = 0V, T=25 °C			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, Pin 5 to Pin 2	6		10	V
Forward Voltage	V_F	I_F = 15mA, T=25 °C, Pin 2 to Pin 5		0.8	1	V
ESD Clamping Voltage –I/O	V_{clamp_io}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground		12		V
ESD Clamping Voltage –VDD	V_{clamp_VDD}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, VDD pin to Ground		9		V
ESD Dynamic Turn on Resistance –I/O	$R_{dynamic\_io}$	IEC 61000-4-2 0~+6kV,T=25 °C, Contact mode,Any Channel pin to Ground		0.3		
ESD Dynamic Turn on Resistance –VDD	$R_{dynamic\_VDD}$	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, VDD pin to Ground		0.14		
Lightning Clamping Voltage	$V_{lightning}$	I_{PP}=4.7A, tp=8/20 s, T=25 °C Any Channel pin to Ground		8.5		V
Channel Input Capacitance -1	C_{IN-1}	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, Any Channel pin to Ground		0.55	0.65	pF
Channel Input Capacitance - 2	C_{IN-2}	**V_{pin5}=floated**,V_{pin2}=0V,**V_{IN}=2.5V**,f=1MHz,T=25°C,Any Channel pin to Ground		0.7	0.9	pF
Channel to Channel Input Capacitance -1	$C_{CROSS-1}$	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , Between Channel pins		0.03	0.06	pF
Channel to Channel Input Capacitance -2	$C_{CROSS-2}$	**V_{pin5} =floated**,V_{pin2} =0V,**V_{IN} =2.5V**,f =1MHz,T=25 °C,Between Channel pins		0.05	0.08	pF
Variation of Channel Input Capacitance -1	$\triangle C_{IN-1}$	**V_{pin5} =5V**, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.03	0.06	pF
Variation of Channel Input Capacitance -2	$\triangle C_{IN-2}$	**V_{pin5} =floated**, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.05	0.08	pF

4.3. TYPICAL CHARACTERISTICS

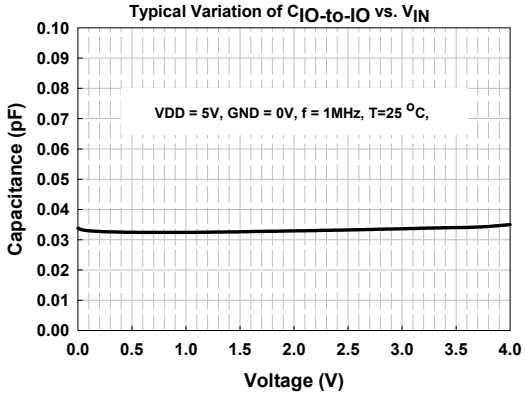
Typical Variation of C_{IN} vs. V_{IN}



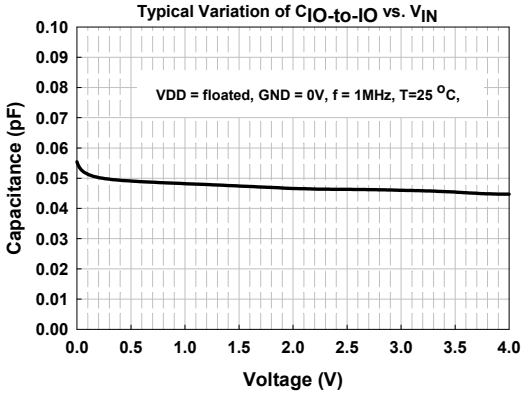
Typical Variation of C_{IN} vs. V_{IN}



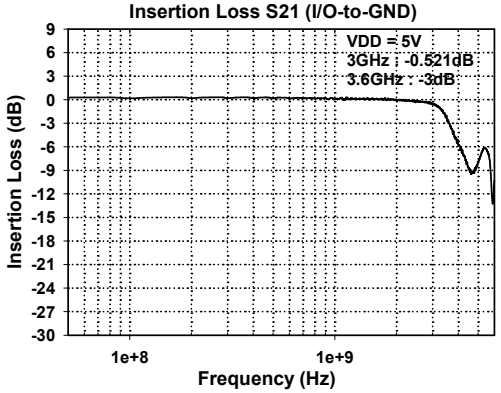
Typical Variation of $C_{IO\text{-}to\text{-}IO}$ vs. V_{IN}



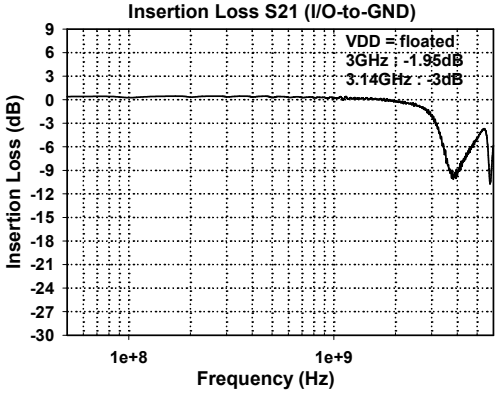
Typical Variation of $C_{IO\text{-}to\text{-}IO}$ vs. V_{IN}



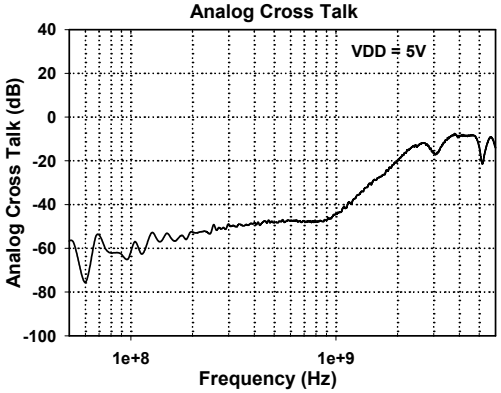
Insertion Loss S21 (I/O-to-GND)



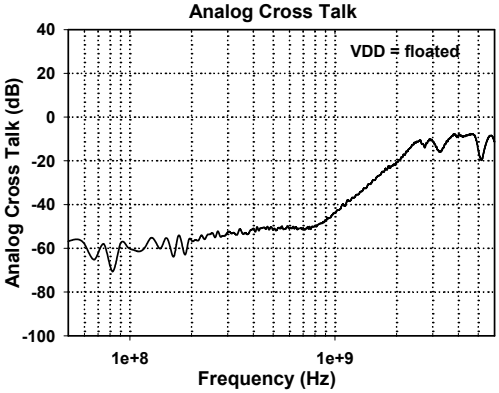
Insertion Loss S21 (I/O-to-GND)

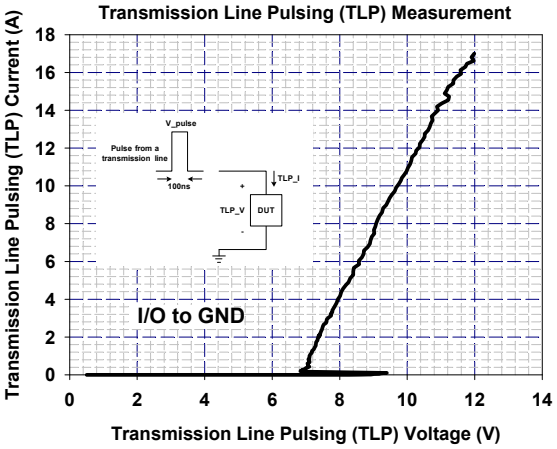


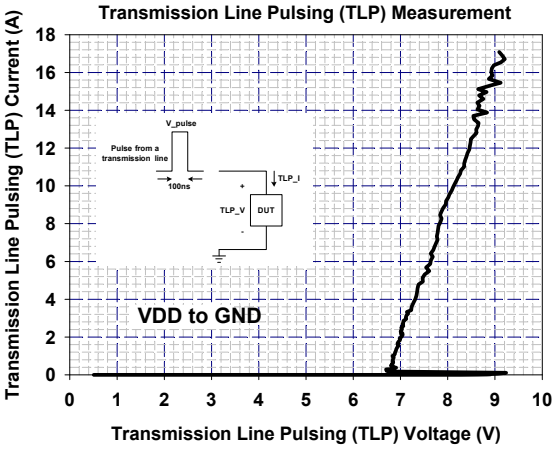
Analog Cross Talk



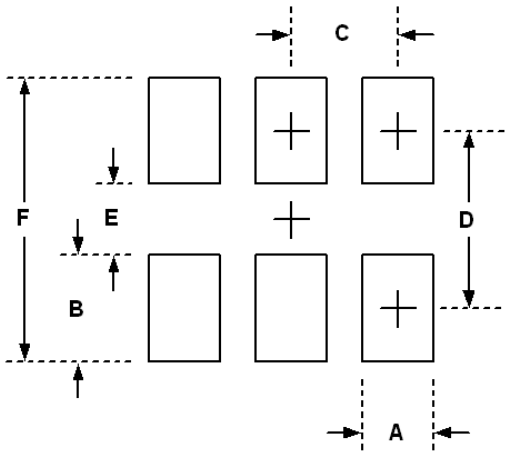
Analog Cross Talk







5. LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

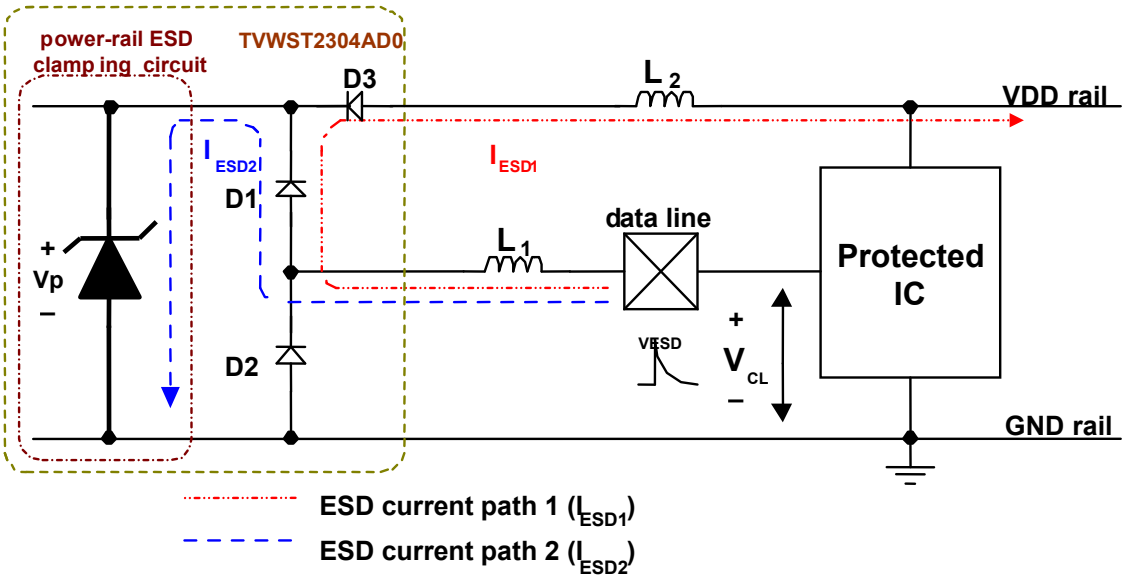
6. Application information

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

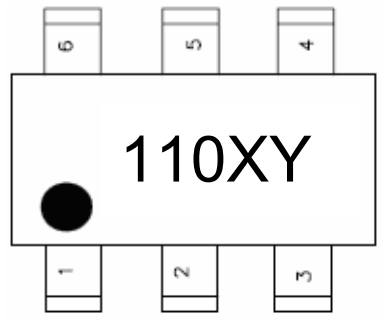
Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail. An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or 30/(1x10-9). So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The TVW ST23 04 AD0 has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.



7. MARKING CODE

Marking Code: 110XY

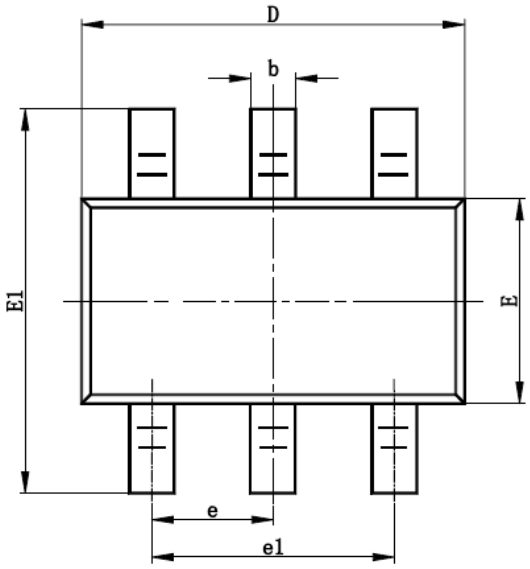


110 = Device Code
X = Date Code
Y = Control Code

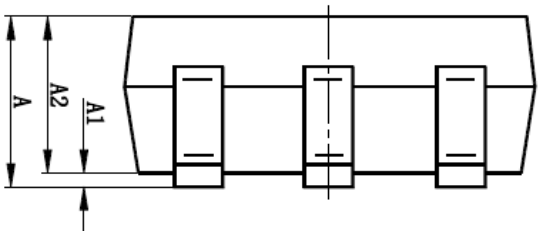
8. Mechanical Details

SOT23-6L PACKAGE DIAGRAMS

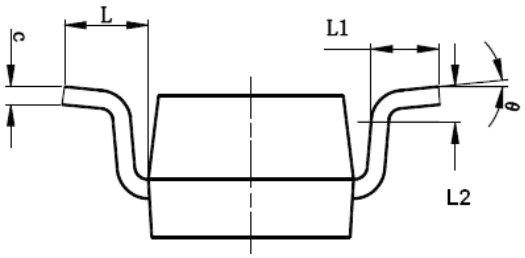
TOP VIEW



SIDE VIEW



END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0	0.15	0.000	0.006
A2	0.9	1.3	0.035	0.051
b	0.3	0.5	0.012	0.020
c	0.08	0.21	0.003	0.008
D	2.72	3.12	0.107	0.123
E	1.4	1.8	0.055	0.071
E1	2.6	3	0.102	0.118
e	0.95BSC		0.037BSC	
e1	1.9BSC		0.075BSC	
L1	0.3	0.6	0.012	0.024
L	0.7REF		0.028REF	
L2	0.25BSC		0.010BSC	
□	0	8	0	8

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters, and the dimensions in inches are for reference only.
- 1mm = 40 mils = 0.04 inches.